REMARKS

Claims 1 through 4, 6 through 12, 14 through 29, 31 through 37, and 39 through 45 are currently pending in the application.

Claims 5, 13, 30, and 38 have been canceled.

Claims 7, 21, 23 and 32 are withdrawn from consideration as being directed to non-elected inventions.

This amendment is in response to the Office Action of June 15, 2005.

Supplemental Information Disclosure Statements

Please note that Supplemental Information Disclosure Statements were filed herein on May 21, 2004 and November 2, 2004, and that no copies of the PTO-1449 forms were returned with the outstanding Office Action. Applicants respectfully request that the information cited on the PTO-1449 forms be made of record herein. For the sake of convenience, second copies of the May 21, 2004 and November 2, 2004, Supplemental Information Disclosure Statements, PTO-1449 forms, and USPTO date-stamped postcards are enclosed herewith. It is respectfully requested that initialed copies of the PTO-1449 forms evidencing consideration of the cited references be returned to the undersigned attorney.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on Marrs (U.S. Patent No. 5,701,034)

Claims 1, 2, 4, 6, 8 through 12, 14 through 20, 24 through 27, 29, 31, 33 through 37, and 39 through 45 were rejected under 35 U.S.C. § 102(b) as being anticipated by Marrs (U.S. Patent 5,701,034).

Applicants assert that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over the cited prior art.

Applicants assert that the claimed inventions of presently amended independent claims 1, 24, and 25 are not anticipated by the Marrs reference under 35 U.S.C. § 102 because Marrs does not identically describe the claimed invention in as complete detail as contained in the claims.

Marrs describes or teaches or suggests a packaged integrated circuit including a heat sink with a locking moat. (Col. 5, lines 1-3). A semiconductor die is attached to a surface of a heat sink using adhesive. (Col. 5, lines 6-8). Package leads are attached to the heat sink also using adhesive. (Col. 5, lines 15-16). Using conventional bond wiring methods the bond wires are extended between the bond pads on the semiconductor die and the heat sink. (Col. 5, lines 18-24). The die, heat sink, bond wires and inner portions of package leads are encapsulated by molding in encapsulant. (Col. 5, lines 24-28). The encapsulant fills in the locking moat formed in the heat sink and becomes interlocked with the heat sink. (Col. 5, lines 29-32). Additionally, Marrs describes or teaches or suggests a packaged semiconductor die or dice including a heat sink with a locking feature that can be used to support one or more generally conductive layers thereon and insulated from the heat sink to provide a ground plane or planes, power plane or planes, or signal routing. (See FIG. 4, COLUMN 4, Lines 10-13.)

By way of contrast to Marrs, the embodiment of the invention set forth in claim 1 recites elements of the invention calling for an integrated circuit package comprising "an integrated circuit die positioned within the package body", "a lead frame including a plurality of leads having portions enclosed within the package body that connect to the integrated circuit die, the plurality of leads having portions enclosed within the package body forming an area", and "an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body and with a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink under the die-attach area and the integrated circuit die projecting away from the first portion of the heat sink, the heat sink coupled to

from the first portion of the heat sink, the heat sink coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame for reducing lead inductance at least about 0.90 nanoheneries from that of a conventional electrically isolated heat sink". Marrs does not identically describe, either expressly or inherently, an integrated circuit die positioned within the package body, nor does Marrs identically describe, either expressly or inherently, a lead frame having a plurality of leads having portions enclosed within the package body, nor identically describe "an electrically conductive heat sink positioned at least partially within the package body . . . for reducing lead inductance at least about 0.90 nanoheneries from that of a conventional electrically isolated heat sink. Furthermore, Marrs fails to describe, either expressly or inherently, "a second portion of the heat sink projecting away from the first portion of the heat sink under the die-attach area".

In Marrs the package body 101 is covered with an encapsulant 120. (FIG. 1, Col. 5, lines 3-4). The leads 102 are external to the integrated circuit or semiconductor die and are attached to heat sink 110 using adhesive 118. (Col. 5, lines 13-15) and are partially covered with encapsulant 120.

Furthermore, Marrs does not identically describe, either expressly or inherently, "an electrically conductive heat sink". Marrs description sets forth that the packaged integrated circuit 200 may be placed on a conductive layer 206, which is sandwiched in between dielectric layers 204 and 208, which are formed around the periphery of the die 101. (Col. 5, lines 34-42). The Applicants' invention incorporates a conductive or ground plane property into the heat sink itself, not the underlying substrate, for reducing lead inductance at least about 0.90 nanoheneries from that of a conventional electrically isolated heat sink. Thus, Marrs does not identically describe the elements of Applicants' presently claimed inventions of presently amended independent claim 1.

Additionally, Marrs does not describe either explicitly or inherently "a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink projecting away from the first portion of the heat sink." Marrs describes a single piece heat sink 110 having a locking moat 112. (FIG. 1). Since Marrs describes only a single piece heat sink,

single piece heat sink, Marrs cannot describe a second portion projecting away from the first portion of the heat sink.

As Marrs fails to expressly or inherently identically describe every element of claim 1, Applicants submit that claim 1 is not anticipated by Marrs under 35 U.S.C. § 102.

Claims 2, 4, 6, 8 through 12, and 14 through 20 are allowable as either directly or indirectly from allowable claim 1.

Independent claim 24 is allowable as Marrs does not describe "an electrically conductive heat sink positioned at least partially within the package body with a vertically extending columnar portion surrounded by a horizontally extending skirt portion having a vertical thickness, said columnar portion having a vertical thickness which is greater than the vertical thickness of said skirt portion, and having a lead frame attachment surface proximate a die-attach surface substantially vertically aligned with the columnar portion, the lead frame attachment surface being attached to the lead frame and extending in close proximity to a substantial part of the enclosed portions of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body, the die-attach surface being attached to the integrated circuit die for reducing lead inductance at least about 0.90 nanoheneries from that of a conventional electrically isolated heat sink". Marrs discloses a one-piece heat sink 110. (FIG. 1). Furthermore, the heat sink in Marrs does not vary in thickness, rather, there is only a slot formed in a portion thereof. (FIGs. 1, 2A, 2B, 4, 8). Additionally, Marrs does not identically describe, either expressly or inherently, a conductive or ground plane property into the heat sink itself for reducing lead inductance at least about 0.90 nanoheneries from that of a conventional electrically isolated heat sink. Since Marrs fails to identically describe, either expressly or inherently, each and every element of claim 24, Applicants respectfully submits that claim 24 is not anticipated by Marrs under 35 U.S.C. § 102.

Independent claim 25 is allowable as Marrs does not identically describe, either expressly or inherently "an electrically conductive heat sink positioned having a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of an enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion

die, a second portion of the heat sink under the die-attach area and the integrated circuit die projecting away from the first portion of the heat sink, the heat sink coupled to one of a signal voltage and a reference voltage for the heat sink to operate respectively as a signal plane and a ground plane for the plurality of leads of the lead frame for reducing lead inductance at least about 0.90 nanoheneries from that of a conventional electrically isolated heat sink. Marrs describes that the packaged integrated circuit 200 may be placed on a conductive layer 206, which is sandwiched in between dielectric layers 204 and 208, which are formed around the periphery of the die 101 and are external to the heat sink. (Col. 5, lines 34-42). The Applicants' invention incorporates a conductive or ground plane property into the heat sink itself, not the underlying substrate. Marrs fails to identically describe the Applicants presently claimed invention having a conductive or ground plane property into the heat sink itself, not the underlying substrate for reducing lead inductance at least about 0.90 nanoheneries from that of a conventional electrically isolated heat sink. Marrs fails to identically describe each and every element of claim 25, Applicant respectfully submits that claim 25 is not anticipated by Marrs under 35 U.S.C. § 102.

Applicants assert that claims 26 through 29, 31, 33 through 37, 39 through 45 are each allowable as depending either directly or indirectly from allowable claim 25.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Marrs (U.S. Patent No. 5,701,034)

Claims 1, 2, 4, 6, 8 through 12, 14 through 20, 24 through 27, 29, 31, 33 through 37, and 39 through 45 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Marrs (U.S. Patent 5,701,034). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants assert that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable

reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

After considering the cited prior art, the rejection, and the Examiner's comments, Applicants have amended the claimed inventions to clearly distinguish over the cited prior art.

Applicants assert that Marrs does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 because Marrs fails to teach or suggest all of the claim limitations and that the rejection is based solely upon Applicants' disclosure, not the cited prior art, because the cited prior art contains no suggestion whatsoever for any such claim limitations.

Marrs teaches or suggests a packaged integrated circuit including a heat sink with a locking moat. (Col. 5, lines 1-3). A semiconductor die is attached to a surface of a heat sink using adhesive. (Col. 5, lines 6-8). Package leads are attached to the heat sink also using adhesive. (Col. 5, lines 15-16). Using conventional bond wiring methods the bond wires are extended between the bond pads on the semiconductor die and the heat sink. (Col. 5, lines 18-24). The die, heat sink, bond wires and inner portions of package leads are encapsulated by molding in encapsulant. (Col. 5, lines 24-28). The encapsulant fills in the locking moat formed in the heat sink and becomes interlocked with the heat sink. (Col. 5, lines 29-32). Additionally, Marrs describes or teaches or suggests a packaged semiconductor die or dice including a heat sink with a locking feature that can be used to support one or more generally conductive layers thereon and insulated from the heat sink to provide a ground plane or planes, power plane or planes, or signal routing. (See FIG. 4, COLUMN 4, Lines 10-13.)

By way of contrast to Marrs, the embodiment of the invention set forth in claim 1 recites elements of the invention calling for an integrated circuit package comprising "an integrated circuit die positioned within the package body", "a lead frame including a plurality of leads having portions enclosed within the package body that connect to the integrated circuit die, the plurality of leads having portions enclosed within the package body forming an area", and "an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body and with a die-attach area on the surface of the first portion of the heat sink attached

the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink under the die-attach area and the integrated circuit die projecting away from the first portion of the heat sink, the heat sink coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame for reducing lead inductance at least about 0.90 nanoheneries from that of a conventional electrically isolated heat sink". Marrs does not teach or suggest the claim limitations calling for an integrated circuit die positioned within the package body, nor does Marrs identically describe, either expressly or inherently, a lead frame having a plurality of leads having portions enclosed within the package body, nor identically describe "an electrically conductive heat sink positioned at least partially within the package body . . . for reducing lead inductance at least about 0.90 nanoheneries from that of a conventional electrically isolated heat sink. Furthermore, Marrs fails to teach or suggest the claim limitations calling for "a second portion of the heat sink projecting away from the first portion of the heat sink under the die-attach area".

In Marrs the package body 101 is covered with an encapsulant 120. (FIG. 1, Col. 5, lines 3-4). The leads 102 are external to the integrated circuit or semiconductor die and are attached to heat sink 110 using adhesive 118. (Col. 5, lines 13-15) and are partially covered with encapsulant 120.

Furthermore, Marrs does not teach or suggest the claim limitations calling for "an electrically conductive heat sink". Marrs description sets forth that the packaged integrated circuit 200 may be placed on a conductive layer 206, which is sandwiched in between dielectric layers 204 and 208, which are formed around the periphery of the die 101. (Col. 5, lines 34-42). The Applicants' invention incorporates a conductive or ground plane property into the heat sink itself, not the underlying substrate, for reducing lead inductance at least about 0.90 nanoheneries from that of a conventional electrically isolated heat sink. Thus, Marrs does not each or suggest the claim limitations of Applicants' presently claimed invention of presently amended independent claim 1.

Additionally, Marrs does not teach or suggest the claim limitations calling for "a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink projecting away from the first portion of the heat sink." Marrs describes a single piece heat sink 110 having a locking moat 112. (FIG. 1). Since Marrs describes only a single piece heat sink, Marrs cannot describe a second portion projecting away from the first portion of the heat sink.

As Marrs fails to teach or suggest the claim limitations of presently amended independent claim 1, Applicants submit that Marrs fails to establish a *prima facie* case of obviousness under 35 U.S.C. § 103.

Claims 2, 4, 6, 8 through 12, and 14 through 20 are allowable as either directly or indirectly from allowable claim 1.

Independent claim 24 is allowable as Marrs does not teach or suggest the claim limitations calling for "an electrically conductive heat sink positioned at least partially within the package body with a vertically extending columnar portion surrounded by a horizontally extending skirt portion having a vertical thickness, said columnar portion having a vertical thickness which is greater than the vertical thickness of said skirt portion, and having a lead frame attachment surface proximate a die-attach surface substantially vertically aligned with the columnar portion, the lead frame attachment surface being attached to the lead frame and extending in close proximity to a substantial part of the enclosed portions of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body, the die-attach surface being attached to the integrated circuit die <u>for reducing lead inductance at least about 0.90 nanoheneries from that of a conventional electrically isolated heat sink</u>". Marrs teaches or suggests a one-piece heat sink 110. (FIG. 1). Furthermore, the heat sink in Marrs does not vary in thickness, rather, there is only a slot formed in a portion thereof. (FIGs. 1, 2A, 2B, 4, 8). Additionally, Marrs does not teach or suggest the claim limitations calling for a conductive or ground plane property into the heat sink itself <u>for reducing lead inductance at least about 0.90 nanoheneries from that of a conventional electrically isolated heat sink</u>. Since Marrs fails to teach or suggest the claim limitations of presently amended independent claim 24, Applicants respectfully submits that Marrs dopes not establish *a prima facie* case of obviousness under

facie case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention. Independent claim 25 is allowable as Marrs does not teach or suggest the claim limitations calling for "an electrically conductive heat sink positioned having a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of an enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink under the die-attach area and the integrated circuit die projecting away from the first portion of the heat sink, the heat sink coupled to one of a signal voltage and a reference voltage for the heat sink to operate respectively as a signal plane and a ground plane for the plurality of leads of the lead frame for reducing lead inductance at least about 0.90 nanoheneries from that of a conventional electrically isolated heat sink. Marrs teaches or suggests that the packaged integrated circuit 200 may be placed on a conductive layer 206, which is sandwiched in between dielectric layers 204 and 208, which are formed around the periphery of the die 101 and are external to the heat sink. (Col. 5, lines 34-42). The Applicants' invention incorporates a conductive or ground plane property into the heat sink itself, not the underlying substrate. Marrs fails to teach or suggest the Applicants presently claimed invention having a conductive or ground plane property into the heat sink itself, not the underlying substrate for reducing lead inductance about 0.90 nanoheneries from that of a conventional electrically isolated heat sink. Marrs fails to teach or suggest the claim limitations of presently amended independent claim 25. Applicants respectfully submit that Marrs does not establish a *prima faice* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention.

Applicants assert that claims 26 through 29, 31, 33 through 37, 39 through 45 are each allowable as depending either directly or indirectly from allowable claim 25.

Applicants assert that the solely basis for the assertions that the claim limitations are present in the cited prior art is the Applicants' disclosure, not the cited prior art, as the Office Action states that such claim limitations are not taught or suggested by the cited prior art. Applicants further assert that the level of skill in the prior art cannot be relied upon t provide the suggestion for the invention. The Office Action speculates that it would be an obvious matter of design choice by well known manufacturing constrains and ascertainable by routine experimentation and optimization to choose the

experimentation and optimization to choose the particular area percentage and columnar portion and skirt relative thicknesses. Such an assertion regarding the claimed invention is within the capabilities of one of ordinary skill in the art in not sufficient by itself to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention.

Obviousness Rejection Based on Marrs (U.S. Patent 5,701,034) as applied to claims 1, 2, 4-6, 8-20, 24-27, 29-31 and 33-45, and further in combination with Wark (U.S. Patent 5,696,031)

Claims 3, 22 and 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Marrs (U.S. Patent 5,701,034) as applied to claims 1, 2, 4-6, 8-20, 24-27, 29-31 and 33-45, and further in combination with Wark (U.S. Patent 5,696,031). Applicants respectfully traverse this rejection, as hereinafter set forth.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over the cited prior art.

Again, Applicants assert submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Applicants assert that Marrs does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 because Marrs fails to teach or suggest all of the claim limitations and that the rejection is based solely upon Applicants' disclosure, not the cited prior art, because the cited prior art contains no suggestion whatsoever for any such claim limitations.

Marrs teaches or suggests a packaged integrated circuit including a heat sink with a locking moat. (Col. 5, lines 1-3). A semiconductor die is attached to a surface of a heat sink using adhesive. (Col. 5, lines 6-8). Package leads are attached to the heat sink also using adhesive. (Col. 5, lines 15-16).

(Col. 5, lines 15-16). Using conventional bond wiring methods the bond wires are extended between the bond pads on the semiconductor die and the heat sink. (Col. 5, lines 18-24). The die, heat sink, bond wires and inner portions of package leads are encapsulated by molding in encapsulant. (Col. 5, lines 24-28). The encapsulant fills in the locking moat formed in the heat sink and becomes interlocked with the heat sink. (Col. 5, lines 29-32). Additionally, Marrs describes or teaches or suggests a packaged semiconductor die or dice including a heat sink with a locking feature that can be used to support one or more generally conductive layers thereon and insulated from the heat sink to provide a ground plane or planes, power plane or planes, or signal routing. (See FIG. 4, COLUMN 4, Lines 10-13.)

Wark teaches or suggests a device and method for stacking wire-bonded integrated circuit dice on flip-chip bonded integrated circuit dice. In addition, Wark teaches or suggests a multi-chip module which is incorporated into a memory device and forms part of an electronic system that includes an input device, an output device, and a processor. The multi-chip module may be incorporated into any of the devices in the module. (Col. 5, lines 59-65).

Applicants respectfully submit that that any combination of Marrs and Wark fail to teach or suggest the claim limitations of presently amended independent claims 1, 22, and 25 to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claim limitations of the presently claimed invention of presently amended independent claim 22 calling for "a package body", "an integrated circuit die positioned within the package body", "a lead frame including a plurality of leads having portions enclosed within the package body that connect to the integrated circuit die, the plurality of leads having portions enclosed within the package body forming an area", and "an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of at least eighty percent of the area formed by the plurality of leads of the lead frame having portions enclosed within the package body forming an area and having a die-attach area on the surface of the first portion of the heat sink attached to the integrated circuit die, a second portion of the heat sink under the die-attach area and the integrated circuit die projecting away from the first portion of the

area and the integrated circuit die projecting away from the first portion of the heat sink and the integrated circuit die for reducing lead inductance at least about 0.90 nanoheneries from that of a conventional electrically isolated heat sink"."

Further, in contrast to the presently claimed invention of presently amended independent claim 22, Applicants assert that Marrs teaches or suggests a one-piece heat sink construction as discussed above which is clearly not the Applicants presently claimed inventions. Wark teaches or suggests stacking the integrated circuit dice to achieve greater component density in the construction of an electronic system.

Applicants submit that the references themselves teach away from any proposed combination thereof and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention of presently amended independent claim 22 since Marrs teaches or suggests preventing delamination of the encapsulating material. Wark teaches away from mounting integrated circuit devices on heat sinks, since stacking would prevent the heat sinks from operating effectively and would transfer heat to the lower component in the stack. Applicants assert that it would not be obvious to combine a method for stacking heat generating integrated circuit devices (Wark) with a method of interlocking encapsulant with a heat sink of Marrs since to do so would destroy the invention of Marrs.

Accordingly, for the reasons herein, Applicants assert that any combination of Marrs and Wark cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention of presently amended independent claim 22.

Claims 3 and 28 are each allowable as depending, either directly or indirectly from allowable presently amended claim 22 and 25 respectively.

Applicants request entry of this amendment for the following reasons:

The amendment is timely filed.

The amendment does not require any further search or consideration.

The amendment places the application in condition for allowance.

Applicants submit that claims 1 through 4, 6, 8 through 12, 14 through 20, 22, 24 through 29, 31, 33 through 37, and 39 through 45 are clearly allowable over the cited prior art.

Applicants request the entry of this amendment, the allowance of claims 1 through 4, 6, 8 through 12, 14 through 20, 22, 24 through 29, 31, 33 through 37, and 39 through 45, and the case passed for issue.

Respectfully submitted,

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Date: August 15, 2005
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